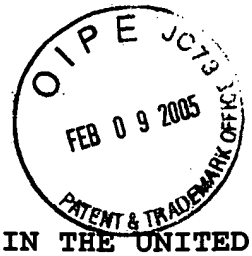

Patent Application
Attorney Docket No.: 57941.000060
Client Reference No.: RA171.CIP1.D1.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
	:	
Belgacem Haba et al.	:	Group Art Unit: 2841
	:	
Appln. No.: 10/695,854	:	
	:	Examiner: H. Bui
Filed: October 30, 2003	:	
	:	
	:	
For: MULTIPLE CHANNEL MODULES AND BUS SYSTEMS USING SAME	:	

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF ISSUE FEE AND PUBLICATION FEE TRANSMITTAL

Sir:

Submitted herewith is the Part B - Issue Fee Transmittal for the above-identified patent application.

[ ] No additional fee is required.

[X] Also attached: Comments on Examiner's Statement of Reasons for Allowance, Change of Maintenance Fee Address, Check in the amount of $1700.00, and Return Receipt Postcard.

[X] The fee is calculated as shown below:

	PRESENT # OF CLAIMS	HIGHEST # PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	24	24	0	x $50 =	$.00
Independent Claims	4	4	0	x $200 =	$.00
				Subtotal	$.00
				Issue Fee	$1400.00
				Subtract ½ if Small Entity	$.00
				Publication Fee	$300.00
				TOTAL FEE DUE	$1700.00

[ ] Please charge Deposit Account No. 50-0206 in the amount of $.00 for the above-indicated fees. A duplicate copy of this transmittal is submitted herewith.

[X] The Commissioner is hereby authorized to charge any shortage in fees associated with the filing of this communication, or credit any overpayment, to Deposit Account No. 50-0206. A duplicate copy of this transmittal is submitted herewith.

Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

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Facsimile: (202) 778-2201

Date: February 9, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
	:	
Belgacem Haba et al.	:	
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Appln. No.: 10/695,854	:	Group Art Unit: 2841
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Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Sir:

In response to the Notice of Allowability dated November 22, 2004, Applicants respectfully submit the following comments regarding the Examiner's statement of reasons for allowance of the above-identified patent application.

In the Notice of Allowability, the Examiner states that "they do not disclose or render obvious in combination between Gulchenski and Zeng et al. as the specific arranged of first and second set of internal buses in the printed circuit board as the claimed invention."

It is respectfully submitted that the foregoing statement by the Examiner is not clear as to the deficiencies of the cited

prior art references with respect to the claimed invention. Thus, Applicants would like to clearly set forth for the record that the cited prior art references, either alone or in combination, do not claim, disclose, or even suggest the claimed invention. Specifically, Applicants would like to clearly set forth for the record that the cited prior art references, either alone or in combination, do not claim, disclose, or even suggest a module having first and second primary surfaces and having a first end, the module comprising: a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces; a first set of input finger connectors disposed on at least one of the first and second primary surfaces; a second set of input finger connectors disposed on at least one of the first and second primary surfaces; a first terminator disposed on at least one of the first and second primary surfaces; a second terminator disposed on at least one of the first and second primary surfaces; a first bus including a first channel extending from the first set of input finger connectors to the first terminator, the first bus connected to a first IC of the plurality of ICs; and a second bus including a second channel extending from the second set of input finger connectors to the second terminator, the second bus connected to a second IC of the plurality of ICs.

Applicants would also like to clearly set forth for the record that the cited prior art references, either alone or in combination, do not claim, disclose, or even suggest a module having first and second primary surfaces and having a first end, the module comprising: a first integrated circuit (IC) populating at least one of the first and second primary surfaces; a first set of input finger connectors disposed on at least one of the first and second primary surfaces; a first set of output finger connectors disposed on at least one of the first and second primary surfaces; a second set of input finger connectors disposed on at least one of the first and second primary surfaces; a terminator disposed on at least one of the first and second primary surfaces; a first bus including a first channel extending from the first set of input finger connectors to the first set of output finger connectors, the first bus connected to the first IC; and a second bus including a second channel extending from the second set of input finger connectors to the terminator.

Applicants would further like to clearly set forth for the record that the cited prior art references, either alone or in combination, do not claim, disclose, or even suggest a module having first and second primary surfaces and having a first end, the module comprising: a plurality of integrated circuits (ICs)

populating at least one of the first and second primary surfaces; first input connector means disposed on at least one of the first and second primary surfaces; second input connector means disposed on at least one of the first and second primary surfaces; first terminator means disposed on at least one of the first and second primary surfaces; second terminator means disposed on at least one of the first and second primary surfaces; first bus means including a first channel extending from the first input connector means to the first terminator means, the first bus means connected to a first IC of the plurality of ICs; and second bus means including a second channel extending from the second input connector means to the second terminator means, the second bus means connected to a second IC of the plurality of ICs.

Applicants would additionally like to clearly set forth for the record that the cited prior art references, either alone or in combination, do not claim, disclose, or even suggest a module having first and second primary surfaces and having a first end, the module comprising: a first integrated circuit (IC) populating at least one of the first and second primary surfaces; first input connector means disposed on at least one of the first and second primary surfaces; first output connector means disposed on at least one of the first and second primary

surfaces; second input connector means disposed on at least one of the first and second primary surfaces; terminator means disposed on at least one of the first and second primary surfaces; first bus means including a first channel extending from the first input connector means to the first output connector means, the first bus means connected to the first IC; and second bus means including a second channel extending from the second input connector means to the terminator means.

In view of the foregoing, it is respectfully submitted that the present application is in condition for issuance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

HUNTON & WILLIAMS LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

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Date: February 9, 2005